AMENDMENT TO THE CLAIMS

This listing of claims will replace all prior versions of claims in the application.

Listing of Claims:

1. (currently amended) An apparatus comprising:

a converter circuit, including a first pair of complementary metal-oxide-semiconductor (CMOS) transistors coupled to be gated by ~~having~~ a dynamic logic input signal, ~~and configured~~ to generate a static logic output signal on an output node responsive to the dynamic logic input signal during an evaluate phase of a clock signal, the static logic output signal having a first state or a second state depending on the dynamic logic input signal, the converter circuit further including a first clocked transistor to enable the first pair of CMOS transistors during the evaluate phase, but to float the output node to retain the state of the static logic output signal during a precharge phase of the clock signal when a precharge voltage is to be applied to gate inputs of the first pair of CMOS transistors; and

a noise suppression circuit, including a second pair of CMOS transistors coupled to ~~receive a clock signal and coupled to the output node, wherein a precharge of a dynamic logic circuit generating the dynamic logic input occurs responsive to a first phase of the clock signal, and wherein the noise suppression circuit is configured to actively drive the static logic output on the output node responsive to the first phase~~ be gated by a feedback voltage from the output node, to sustain the state of the output node during the precharge phase, the noise suppression circuit further including a second clocked transistor which is to be enabled during the precharge phase to couple a first potential onto the output node through the second clocked transistor and one of the second pair of CMOS transistors when the output node is in the first state, but to couple a second potential through the other of the second pair of CMOS transistors and one of the first pair of CMOS transistors of the converter circuit when the output node is in the second state.

2. (currently amended) The apparatus as recited in claim 1 wherein the ~~converter circuit~~

~~is coupled to receive the clock signal and to generate the static logic output further responsive to~~ first clocked transistor is to be active during the evaluate phase of the clock signal and the second clocked transistor is to be active during the precharge phase of the clock signal.

3. (currently amended) The apparatus as recited in claim 2 wherein the converter circuit is coupled to receive a plurality of dynamic logic inputs ~~including the dynamic logic input~~ signals, and wherein the static logic output signal is a logical combination of the plurality of dynamic logic inputs signals.

4. (currently amended) The apparatus as recited in claim ~~1 wherein the noise suppression circuit is coupled to the converter circuit, and wherein the noise suppression circuit is configured to actively drive the static logic output through one or more transistors in the converter circuit~~ 2 wherein the first clocked transistor is a NMOS transistor and the second clocked transistor is a PMOS transistor.

5. (currently amended) The apparatus as recited in claim ~~1 wherein the noise suppression circuit is coupled to receive a feedback signal corresponding to the static logic output, wherein the noise suppression circuit is configured to actively drive the static logic output further responsive to the feedback signal~~ 2 wherein the first potential placed on the output node is coupled from a supply voltage and the second potential placed on the output node is coupled from ground.

6. (currently amended) The apparatus as recited in claim 5 ~~further comprising an inverter coupled to the output node and to provide the feedback signal~~ wherein the converter circuit operates as an inverter.

7. (currently amended) The apparatus as recited in claim ~~5 wherein the noise suppression circuit comprises a tristate inverter circuit coupled to receive the feedback signal and coupled to the output node, wherein a tristate control of the tristate inverter circuit is controlled by the clock signal~~ 6 wherein the feedback voltage is an inverted

state of the static logic output signal.

8-9. (canceled)

10. (currently amended) The apparatus as recited in claim ~~8~~ 1 wherein ~~a size of the first transistor and the second transistor is~~ the transistors of the noise suppression circuit are sized between ~~about~~ approximately 30%-50% of ~~a size of~~ the transistors in the converter circuit.

11. (currently amended) The apparatus as recited in claim ~~8~~ 1 wherein ~~a size of the first transistor and the second transistor is about~~ the transistors of the noise suppression circuit are sized approximately 30% of ~~a size of~~ the transistors in the converter circuit.

12. (currently amended) The apparatus as recited in claim ~~8~~ 1 wherein ~~a size of the first transistor and the second transistor is selected~~ the transistors of the converter circuit and the noise suppression circuit are sized according to an expected noise on the output node.

13. (currently amended) A circuit ~~for actively driving an output node on which a static logic signal corresponding to a dynamic logic signal is supplied via a converter circuit, the circuit~~ comprising:

~~a first transistor having a first node, a second node, and a first control node, wherein the first node is coupled to a power supply and the first control node is coupled to receive a feedback signal corresponding to the static logic signal; and~~

~~a second transistor having a third node connected to the second node, a fourth node connected to the output node, and a second control node controlled by the clock signal, wherein a precharge of a dynamic logic circuit generating the dynamic logic input occurs responsive to a first phase of the clock signal, and wherein the second transistor activates during the first phase responsive to the clock signal~~

a converter circuit having a first pair of complementary metal-oxide-semiconductor (CMOS) transistors and a first clocked transistor coupled in series between a supply voltage node and a supply return node and in which an output node is

obtained at a junction of the first pair of CMOS transistors, the first pair of CMOS transistors coupled to be gated by a dynamic logic input signal to generate a static logic output signal onto the output node during an evaluate phase of a clock signal when the clock signal activates the first clocked transistor to enable the converter circuit, but during a precharge phase of the clock signal when a precharge voltage is to be applied to gate inputs of the first pair of CMOS transistors, the first clocked transistor is deactivated to float the output node to retain existing state of the static logic output signal; and

a noise suppression circuit having a second pair of CMOS transistors and a second clocked transistor, in which one of the second pair of CMOS transistors and the second clocked transistor are coupled in series between the supply voltage node and the output node and other of the second pair of CMOS transistors and one of the transistors of the first pair of CMOS transistors of the converter circuit are coupled in series between the output node and the supply return node, the second pair of CMOS transistors gated by a feedback voltage from the output node to either place a supply voltage potential from the supply voltage node or supply return potential from the supply return node onto the output node during the precharge phase to maintain the state of the static logic output signal to suppress noise on the output node.

14. (currently amended) The circuit as recited in claim 13 ~~further comprising a third transistor having a fifth node coupled to ground, a sixth node, and a third control node controlled by the clock signal, wherein the sixth node is coupled to the converter circuit to form a current path with at least a fourth transistor in the converter circuit which is coupled to receive the dynamic logic input on its control node~~ wherein the first clocked transistor is a NMOS transistor and the second clocked transistor is a PMOS transistor.

15. (currently amended) The circuit as recited in claim 14 wherein the ~~first and second transistors are PMOS transistors and the third transistor is an NMOS transistor~~ one of the second pair of CMOS transistors and the second clocked transistor coupled between the supply voltage node and the output node are PMOS transistors and wherein the other of the second pair of CMOS transistors and one of the transistors of the first pair of CMOS transistors coupled between the output node and the supply return node are NMOS

transistors.

16. (currently amended) The circuit as recited in claim 14 wherein the converter circuit is coupled to receive a plurality of dynamic logic inputs ~~including the dynamic logic input~~ signals, and wherein the ~~converter circuit includes a plurality of transistors including the fourth transistor, each of the plurality of transistors coupled to receive a respective dynamic logic input of the plurality of dynamic logic inputs on its control node, and wherein the third transistor is coupled in series with the plurality of transistors~~ static logic output signal is a logical combination of the plurality of dynamic logic input signals.

17. (currently amended) The circuit as recited in claim ~~16 wherein the plurality of transistors are coupled in parallel with each other~~ 15 wherein the transistors of the noise suppression circuit are sized between approximately 30%-50% of the transistors in the converter circuit.

18. (currently amended) The circuit as recited in claim ~~16 wherein the plurality of transistors are coupled in series with each other~~ 15 wherein the transistors of the noise suppression circuit are sized approximately 30% of the transistors in the converter circuit.

19. (currently amended) A method comprising:

~~generating a static logic output on a node responsive to a dynamic logic input; and~~

~~actively driving the static logic output on the node responsive to a first phase of a clock signal, wherein a precharge of a dynamic logic circuit generating the dynamic logic input occurs responsive to a first phase of the clock signal~~

inputting a dynamic logic signal to convert the dynamic logic signal to a static logic signal;

clocking to convert the dynamic logic signal to the static logic signal during an evaluate phase of a clock signal and output the static logic signal onto an output node;

deactivating conversion of the dynamic logic signal to the static logic signal during a precharge phase of the clock signal to retain a state of the output logic signal on

the output node and preventing a precharge state from being coupled to the output node; and

utilizing a feedback voltage from the output node to activate a path from either a supply voltage node or a supply return node to place a supply voltage potential or a supply return potential on the output node to maintain the state of the output logic signal during the precharge phase of the clock signal, in which one of the paths is through a transistor used to convert the dynamic logic signal to the static logic signal.

20. (currently amended) The method as recited in claim 19 wherein ~~the actively driving is further responsive to a feedback signal corresponding to the static logic output~~ a second path is from the output node to a supply voltage node which is made active during the precharge phase.

21. (currently amended) A computer accessible medium comprising one or more data structures representing one or more of:

a converter circuit, including a first pair of complementary metal-oxide-semiconductor (CMOS) transistors coupled to be gated by ~~having~~ a dynamic logic input signal, ~~and configured~~ to generate a static logic output signal on an output node responsive to the dynamic logic input signal during an evaluate phase of a clock signal, the static logic output signal having a first state or a second state depending on the dynamic logic input signal, the converter circuit further including a first clocked transistor to enable the first pair of CMOS transistors during the evaluate phase, but to float the output node to retain the state of the static logic output signal during a precharge phase of the clock signal when a precharge voltage is to be applied to gate inputs of the first pair of CMOS transistors; and

a noise suppression circuit, including a second pair of CMOS transistors coupled to ~~receive a clock signal and coupled to the output node, wherein a precharge of a dynamic logic circuit generating the dynamic logic input occurs responsive to a first phase of the clock signal, and wherein the noise suppression circuit is configured to actively drive the static logic output on the output node responsive to the first phase~~ be gated by a feedback voltage from the output node, to sustain the state of the output node

during the precharge phase, the noise suppression circuit further including a second clocked transistor which is to be enabled during the precharge phase to couple a first potential onto the output node through the second clocked transistor and one of the second pair of CMOS transistors when the output node is in the first state, but to couple a second potential through the other of the second pair of CMOS transistors and one of the first pair of CMOS transistors of the converter circuit when the output node is in the second state.